L Number	Hits	Search Text	DB	Time stamp
-	0	(716/10).ccls. and (crossbar adj device)	USPAT;	2002/05/23 10:09
			US-PGPUB;	
			EPO; JPO;	
	•		DERWENT;	
	•	(740/0)	IBM_TDB	00000050044400
-	3	(716/\$).ccls. and (crossbar adj device)	USPAT;	2002/05/21 11:30
			US-PGPUB;	
İ			EPO; JPO; DERWENT;	İ
			IBM_TDB	
	91	(716/\$).ccls. and (logic\$ adj interconnect\$)	USPAT;	2002/05/20 17:52
	٠.	(relations and (logist au) interestinesity	US-PGPUB;	2002/00/20 17:02
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	0	(716/\$).ccls. and (logic\$ adj interconnect\$) adj ((pass or	USPAT;	2002/05/20 17:54
		control) adj transistor)	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
	45	dimuon nond monid	IBM_TDB	2002/05/04 00:50
-	15	dimyan near1 magid	USPAT; US-PGPUB;	2002/05/21 09:56
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
_	5226	cross adj connect	USPAT;	2002/05/21 11:22
	4		US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	2	(716/\$).ccls. and (cross adj connect)	USPAT;	2002/05/21 11:23
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
	55	(716/\$).ccls. and (crossbar)	IBM_TDB USPAT;	2002/05/21 12:50
-	55	(710/\$).ccis. and (clossbar)	US-PGPUB;	2002/05/21 12.50
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	538	(716/\$).ccls. and multiplexer	USPAT;	2002/05/21 12:50
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
	400	(716/¢) colo and (multiplesses and decedes)	IBM_TDB	2002/05/24 42:04
-	168	(716/\$).ccls. and (multiplexer and decoder)	USPAT;	2002/05/21 13:04
			US-PGPUB; EPO; JPO;	
			DERWENT;	
			IBM_TDB	
_	21	crossbar and decoder and (pass adj transistor)	USPAT;	2002/05/21 15:40
		(Page and Assessed)	US-PGPUB;	
	i		EPO; JPO;	
			DERWENT;	
			IBM_TDB	
•	21	(crossbar or crossconnect) and decoder and (pass adj	USPAT;	2002/05/21 15:43
		transistor)	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
_	0	crossconnect and decoder and (pass adj transistor)	IBM_TDB USPAT;	2002/05/21 15:43
-	U	orossociment and decoder and (pass adjutansistor)	US-PGPUB;	2002/00/21 10.43
			EPO; JPO;	
ļ			DERWENT;	
ì			IBM_TDB	1

	4540	I decades and force additional and	LIODAT	0000/05/04 40 47
-	1516	decoder and (pass adj transistor)	USPAT;	2002/05/21 16:47
	1		US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
	25	(716/\$).ccls. and decoder and (pass adj transistor)	USPAT;	2002/05/21 16:08
-	25	(7 10/\$).ccis. and decoder and (pass adjuransistor)	US-PGPUB;	2002/03/21 10.06
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
	2	(multiplexer adj type) adj crossbar	USPAT;	2002/05/21 16:29
_	_	(multiplexer adj type) adj crossbar	US-PGPUB;	2002/03/21 10.29
			EPO; JPO;	
	1		DERWENT;	
			IBM_TDB	
_	0	partial adj (crossbar adj connect\$)	USPAT;	2002/05/21 16:36
		partial adj (570000ar adj 5011115514)	US-PGPUB;	2002/00/21 10:00
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	51	decoder and (pass adj transistor) and crossbar	USPAT;	2002/05/21 18:24
			US-PGPUB;	
			EPO; JPO;	'
			DERWENT;	
			IBM_TDB	
-	0	decoder and ((first adj pass) adj transistor) and ((second adj	USPAT;	2002/05/21 18:26
		pass) adj transistor) and crossbar	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	0	((first adj pass) adj transistor) and ((second adj pass) adj	USPAT;	2002/05/21 18:28
		transistor) and crossbar	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	0000005104 40 40
-	30	(pass adj transistor) and chain and crossbar	USPAT;	2002/05/21 18:46
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
	5585	((pass adj transistor) or switch) and crossbar	IBM_TDB USPAT;	2002/05/21 18:48
-	3363	ן (נושפים מען וומוופופוטון טו פאונטון מווע טוטפפטמו	US-PGPUB;	2002/05/21 10.40
			EPO; JPO;	
	ł		DERWENT;	
			IBM_TDB	
_	0	(716/\$).ccls. and (cascade\$ and (pass adj transistor)) and	USPAT;	2002/05/21 18:55
		crossbar	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	0	(716/10).ccls. and latch and (crossbar adj device)	USPAT;	2002/05/22 10:08
		·	US-PGPUB;	
			EPO; JPO;	
1			DERWENT;	
			IBM_TDB	
-	6	latch and (crossbar adj device)	USPAT;	2002/05/22 10:12
			US-PGPUB;	
			EPO; JPO;	
		,	DERWENT;	
1	1		IBM_TDB	0000/05/00 40 54
-	106	latch and mutiplex\$	USPAT;	2002/05/22 10:51
			US-PGPUB;	
	ŀ		EPO; JPO; DERWENT;	
	1		IBM_TDB	,
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] -	1	(716/\$).ccls. and (latch and mutiplex\$)	USPAT;	2002/05/22 11:04
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	148	(716/\$).ccls. and (latch and (input adj data))	USPAT;	2002/05/22 11:21
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
	_		IBM_TDB	
-	6	(716/\$).ccls. and ((input adj data) with switch)	USPAT;	2002/05/22 11:36
	1		US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	1	(716/\$).ccls. and ((input adj data) adj switch)	USPAT;	2002/05/22 11:49
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	3425	(716/\$).ccls. and (input data switch)	USPAT;	2002/05/22 11:51
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	1	(716/\$).ccls. and "input data switch"	USPAT;	2002/05/22 12:00
			US-PGPUB;	
			EPO; JPO;	
•			DERWENT;	
			IBM_TDB	
-	241	"input data switch"	USPAT;	2002/05/22 12:02
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	5	"input data switch" and crossbar	USPAT;	2002/05/22 12:16
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	0	"input data" with "pass adj transistor"	USPAT;	2002/05/22 12:17
			US-PGPUB;	
			EPO; JPO;	
		·	DERWENT;	
			IBM_TDB	000010=100 15 15
-	897	(input adj data) and (pass adj transistor)	USPAT;	2002/05/22 12:19
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
		(740/0)	IBM_TDB	0000/05/00 40 50
-	26	(716/\$).ccls. and (input adj data) and (pass adj transistor)	USPAT;	2002/05/22 13:58
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
		# 4000 TOUR TOUR	IBM_TDB	0000/57/50 15 15
-	1	"4698760".PN.	USPAT	2002/05/22 12:48
-	36	(716/\$).ccls. and (input adj buffer) and (pass adj transistor)	USPAT;	2002/05/22 14:44
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
		(the set and be offered and for any add to a set the set of the se	IBM_TDB	2002/05/02 44:52
-	487	(input adj buffer) and (pass adj transistor)	USPAT;	2002/05/22 14:56
			US-PGPUB;	
			EPO; JPO;	
	1		DERWENT;	
			IBM_TDB	l

US-PGPUB: EPO, JPO; DERWENT: IBM, TDB USPAT; US-PGPUB: EPO, JPO; D					
- 1895 vth and buffer	-	5	memory and ((low adj power) adj structure)	USPAT;	2002/05/22 15:09
- 1895 vth and buffer				,	
IBM_TDB					
1895				1	
- 1 (power adj on) adj reset					
- 1 (power adj on) adj reset	-	1895	vth and buffer		2002/05/22 15:09
DERWENT: IBM_TDB					
1					
1	1				
US-PGPUB: EPO: JPO: DERWENT: IBM. TDB USPAT: US-PGPUB: EPO: JPO:					
Sex POR Sex Sex POR Sex	-	1	(power adj on) adj reset		2002/05/22 15:53
S828 POR DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; DPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; DPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT					
BIM_TDB USPAT; US-PGPUB; EPO.; JPO; DERWENT; BIM_TDB USPAT; US-P			, '		
S828 POR				DERWENT;	
S.P.G.PUB:				IBM_TDB	
POR and (output adj buffer)	-	5828	POR	USPAT;	2002/05/22 15:53
DERWENT: IBM_TDB USPAT: US-PGPUB: EPO; JPO; DERWENT: IBM_TDB USPAT				US-PGPUB;	
DERWENT: IBM_TDB USPAT: US-PGPUB: EPO; JPO; DERWENT: IBM_TDB USPAT					
- 207 POR and (output adj buffer) - 111 POR with (output adj buffer) - 111 POR with (output adj buffer) - 2 POR and (output adj buffer) - 2 POR and (output adj buffer) - 3 ((power adj off) adj reset) and crossbar - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 34 (pass adj transistor) with (input adj buffer) - 70 input adj (pass adj transistor) - 10 ((power adj on) adj reset) with (flip adj flop) - 10 ((power adj on) adj reset) with (flip adj flop) - 11 POR with (output adj buffer) - 12 POR and (output adj buffer) - 2 POR and (output adj buffer) - 2 POR and (output adj buffer) - 3 ((power adj off) adj reset) and crossbar - 3 ((power adj off) adj reset) and crossbar - 3 ((power adj off) adj reset) and crossbar - 3 ((power adj off) adj reset) and coutput adj buffer) - 3 ((power adj off) adj reset) and crossbar - 3 ((power adj off) adj reset) and crossbar - 3 ((power adj off) adj reset) and coutput adj buffer) - 3 ((power adj off) adj reset) and crossbar - 3 ((power adj off) adj reset) and coutput adj buffer) - 3 ((power adj off) adj reset) with (flip adj flop) - 3 ((power adj off) adj reset) with (flip adj flop) - 3 ((power adj off) adj reset) with (flip adj flop) - 3 ((power adj off) adj reset) with (flip adj flop) - 3 ((power adj off) adj reset) with (flip adj flop)					
- 207 POR and (output adj buffer) - 111 POR with (output adj buffer) - 111 POR with (output adj buffer) - 2 POR and (output adj buffer) - 2 POR and (output adj buffer) - 3 ((power adj off) adj reset) and crossbar - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 34 (pass adj transistor) with (input adj buffer) - 70 input adj (pass adj transistor) - 10 ((power adj on) adj reset) with (flip adj flop) - 10 ((power adj on) adj reset) with (flip adj flop) - 11 POR with (output adj buffer) - 12 POR and (output adj buffer) - 2 POR and (output adj buffer) - 2 POR and (output adj buffer) - 3 ((power adj off) adj reset) and crossbar - 3 ((power adj off) adj reset) and crossbar - 3 ((power adj off) adj reset) and crossbar - 3 ((power adj off) adj reset) and coutput adj buffer) - 3 ((power adj off) adj reset) and crossbar - 3 ((power adj off) adj reset) and crossbar - 3 ((power adj off) adj reset) and coutput adj buffer) - 3 ((power adj off) adj reset) and crossbar - 3 ((power adj off) adj reset) and coutput adj buffer) - 3 ((power adj off) adj reset) with (flip adj flop) - 3 ((power adj off) adj reset) with (flip adj flop) - 3 ((power adj off) adj reset) with (flip adj flop) - 3 ((power adj off) adj reset) with (flip adj flop) - 3 ((power adj off) adj reset) with (flip adj flop)				IBM TDB	
- 11 POR with (output adj buffer) - 2 POR and (output adj buffer) - 2 POR and (output adj buffer) and crossbar - 2 POR and (output adj buffer) and crossbar - 0 ((power adj off) adj reset) and (output adj buffer) and crossbar - 0 ((power adj off) adj reset) and (output adj buffer) and crossbar - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 34 (pass adj transistor) with (input adj buffer) - 70 input adj (pass adj transistor) - 1 1 input adj (pass adj transistor) - 1 2 input adj (pass adj transistor) and (mux or multiplexer) - 1 2 input adj (pass adj transistor) and (mux or multiplexer) - 1 3 input adj (pass adj transistor) and (mux or multiplexer) - 1 3 input adj (pass adj transistor) and (mux or multiplexer) - 1 3 input adj (pass adj transistor) and (mux or multiplexer) - 1 3 input adj (pass adj transistor) and (mux or multiplexer) - 1 3 input adj (pass adj transistor) and (mux or multiplexer) - 2 2 input adj (pass adj transistor) and (mux or multiplexer) - 2 3 input adj (pass adj transistor) and (mux or multiplexer) - 2 4 3 input adj (pass adj transistor) and (mux or multiplexer) - 2 5 6 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7 7	-	207	POR and (output adj buffer)		2002/05/22 16:07
POR with (output adj buffer)	1				
DERWENT: IBM TDB USPAT: US-PGPUB; EPO; JPO; DERWENT: IBM TDB USPAT: US-PGPUB; EPO; JPO;	1	}			
IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-	1				
11	1				
US-PGPUB; EPO; JPO; DERWENT; IBM, TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM, TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM, TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM, TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM, TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM, TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM, TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM, TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM, TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM, TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM, TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM, TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM, TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM, TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; US-PGPUB; EPO; JPO; DERW	<u>-</u> '	11	POR with (output adi buffer)		2002/05/23 11:51
POR and (output adj buffer) and crossbar			l ort mar (output au) burior,	· ·	2002/00/20 11:01
- 2 POR and (output adj buffer) and crossbar - 2 POR and (output adj buffer) and crossbar - 0 ((power adj off) adj reset) and (output adj buffer) and crossbar - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 34 (pass adj transistor) with (input adj buffer) - 70 input adj (pass adj transistor) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop) - 2 2 2 2 2 2 2 2 2 16:29 - 2 3 4 2 2002/05/22 16:29 - 2 3 4 2002/05/22 16:29 - 2 3 4 2002/05/22 16:31 - 3 4 2002/05/23 10:11 - 3 5 2002/05/23 10:11 - 2 6 2002/05/23 10:39 - 2 7 6 2002/05/23 10:52 - 2 8 2002/05/23 10:52 - 2 9 2002/05/23 10:52 - 3 6 2002/05/23 10:54 - 3 7 6 2002/05/23 10:54 - 3 8 2002/05/23 10:54 - 4 9 2002/05/23 10:54 - 5 9 2002/05/23 10:54 - 5 9 2002/05/23 10:54 - 5 9 2002/05/23 10:54 - 6 9 2002/05/23 10:54 - 7 9 2002/05/23 10:54 - 7 9 2002/05/23 10:54 - 1 9 2002/05/23 10:54 - 2 1 2 1 2002/05/23 11:20 - 2 1 2 2002/05/23 11:20					
- 2 POR and (output adj buffer) and crossbar - 0 ((power adj off) adj reset) and (output adj buffer) and crossbar - 0 ((power adj off) adj reset) and (output adj buffer) and crossbar - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 34 (pass adj transistor) with (input adj buffer) - 70 input adj (pass adj transistor) - 70 input adj (pass adj transistor) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop)			'		
2 POR and (output adj buffer) and crossbar USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB;					
US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DE	l _	2	POR and (output adi huffer) and crosshar		2002/05/22 16:29
Compared to the content of the con		_	Tork and (output adjounce) and crossoar		2002/00/22 10:20
DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB U					
-					
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- 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 34 (pass adj transistor) with (input adj buffer) - 34 (pass adj transistor) with (input adj buffer) - 70 input adj (pass adj transistor) - 70 input adj (pass adj transistor) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 (2002/05/23 10:54) - 0 (2002/05/23 11:20)		0	((naver adj off) adj react) and (autnut adj huffer) and creeches		2002/05/22 16:21
- 0 (716/\$) ccls. and (pass adj transistor) with (input adj fuffer) - 34 (pass adj transistor) with (input adj buffer) - 34 (pass adj transistor) with (input adj buffer) - 70 input adj (pass adj transistor) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 0 ((power adj on) adj reset) with (flip adj flop) EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	-	0	((power adj oii) adj reset) and (output adj buller) and crossbar	'-	2002/05/22 16:31
- 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 34 (pass adj transistor) with (input adj buffer) - 34 (pass adj transistor) with (input adj buffer) - 70 input adj (pass adj transistor) - 70 input adj (pass adj transistor) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 0 (716/\$).ccls. and (pass adj transistor) - 0 (716/\$).ccls. and (pass a					
- 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT					
- 0 (716/\$).ccls. and (pass adj transistor) with (input adj fuffer) - 34 (pass adj transistor) with (input adj buffer) - 34 (pass adj transistor) with (input adj buffer) - 70 input adj (pass adj transistor) - 70 input adj (pass adj transistor) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop) - 0 ((power adj on) adj reset) with (flip adj flop)		}			
US-PGPUB; EPO; JPO; DERWENT; IBM_TDB US-PGPUB;			(74 C (ft)1		0000/05/00 40:44
PO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; ISM_TDB USPAT; US-PGPUB; EPO; JPO; ISPO; ISP	-	U	(716/\$).ccis. and (pass adj transistor) with (input adj tuffer)		2002/05/23 10:11
- 34 (pass adj transistor) with (input adj buffer) - 70 input adj (pass adj transistor) - 70 input adj (pass adj transistor) - 70 input adj (pass adj transistor) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 22 input adj (pass adj transistor) and (mux or multiplexer) - 34 (pass adj transistor) 2002/05/23 10:39 - 2002/05/23 10:39 - 2002/05/23 10:39 - 2002/05/23 10:52 - 2002/05/23 10:52 - 2002/05/23 10:54 - 35 (pass adj transistor) and (mux or multiplexer) - 36 (pass adj transistor) and (mux or multiplexer) - 37 (pass adj transistor) - 38 (pass adj transistor) - 39 (pass adj transistor) - 30 (pass adj transistor)					
- 34 (pass adj transistor) with (input adj buffer) - 70 input adj (pass adj transistor) - 70 input adj (pass adj transistor) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 0 ((power adj on) adj reset) with (flip adj flop) IBM_TDB		1		EPO; JPO;	
- 34 (pass adj transistor) with (input adj buffer) - 70 input adj (pass adj transistor) - 70 input adj (pass adj transistor) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 0 ((power adj on) adj reset) with (flip adj flop) - USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; USPAT; US-PGPUB; EPO; JPO; USPAT; US-PGPUB; EPO; JPO;		1			
US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; USPAT; US-PGPUB; EPO; JPO; USPAT; US-PGPUB; EPO; JPO; USPAT; US-PGPUB; EPO; JPO; USPAT; US-PGPUB; EPO; JPO; USPAT; US-PGPUB; EPO; JPO; USPAT; US-PGPUB; EPO; JPO; US-PGPUB;	1	1	(many and temperature) with the standard butter A		0000/05/00 40 00
FPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; USPAT; US-PGPUB; EPO; JPO; USPAT; US-PGPUB; EPO; JPO; US-PGPUB; EPO; JPO; DERWENT; US-PGPUB; EPO; JPO; US-PGPUB; EPO; JPO; DERWENT; US-PGPUB; EPO;	-	34	(pass adj transistor) with (input adj buπer)		2002/05/23 10:39
- 70 input adj (pass adj transistor) - 70 input adj (pass adj transistor) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 0 ((power adj on) adj reset) with (flip adj flop) DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; 2002/05/23 10:52					
- 70 input adj (pass adj transistor) input adj (pass adj transistor) 21 input adj (pass adj transistor) and (mux or multiplexer) 12 input adj (pass adj transistor) and (mux or multiplexer) 23 input adj (pass adj transistor) and (mux or multiplexer) 24 input adj (pass adj transistor) and (mux or multiplexer) 25 input adj (pass adj transistor) and (mux or multiplexer) 26 input adj (pass adj transistor) 27 input adj (pass adj transistor) 28 input adj (pass adj transistor) 29 input adj (pass adj transistor) 2002/05/23 10:52 2002/05/23 10:52 2002/05/23 11:20 2002/05/23 11:20					
- 70 input adj (pass adj transistor) USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO;					
- 21 input adj (pass adj transistor) and (mux or multiplexer) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 3 input adj (pass adj transistor) and (mux or multiplexer) - 4 US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; USPAT; US-PGPUB; EPO; JPO;					0000105/00 10 55
EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; USPAT; US-PGPUB; EPO; JPO;	-	70	input adj (pass adj transistor)		2002/05/23 10:52
- 21 input adj (pass adj transistor) and (mux or multiplexer) - 21 input adj (pass adj transistor) and (mux or multiplexer) - 3 USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EVO; JPO; US-PGPUB; EPO; JPO;					
- 21 input adj (pass adj transistor) and (mux or multiplexer) IBM_TDB USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO; USPAT; US-PGPUB; EPO; JPO;		1			
- 21 input adj (pass adj transistor) and (mux or multiplexer) USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EVO; JPO; USPAT; US-PGPUB; EPO; JPO;	1				
US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO;					
EPO; JPO; DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO;	-	21	input adj (pass adj transistor) and (mux or multiplexer)		2002/05/23 10:54
DERWENT; IBM_TDB USPAT; US-PGPUB; EPO; JPO;		1			
- 0 ((power adj on) adj reset) with (flip adj flop) IBM_TDB USPAT; US-PGPUB; EPO; JPO;	1				
- 0 ((power adj on) adj reset) with (flip adj flop) USPAT; 2002/05/23 11:20 US-PGPUB; EPO; JPO;		1			
US-PGPUB; EPO; JPO;	l	1			
EPO; JPO;	-	0	((power adj on) adj reset) with (flip adj flop)		2002/05/23 11:20
		1			
I SERVICE S					
		1		DERWENT;	
IBM_TDB		L		IBM_TDB	

-	1	((power adj on) adj reset) and (flip adj flop)	USPAT;	2002/05/23 11:29
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	1	((power adj on) adj reset)	USPAT;	2002/05/23 11:23
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	0	((power adj on) adj reset) and (output adj buffer)	USPAT;	2002/05/23 11:31
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	1209	(pass adj transistor) and (threshold adj voltage) and memory	USPAT;	2002/05/23 11:55
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	961	(pass adj transistor) and (threshold adj voltage) and memory	USPAT;	2002/05/23 12:12
		and (input and output)	US-PGPUB;	1
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	3	("5282271").PN.	USPAT;	2002/05/23 12:08
			US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
			IBM_TDB	
-	18	(· · · · · · · · · · · · · · · · · · ·	USPAT;	2002/05/23 12:24
		voltage) and memory and (input and output)	US-PGPUB;	
			EPO; JPO;	
			DERWENT;	
•			IBM_TDB	
-	2		USPAT;	2002/05/23 12:26
		voltage) and memory and (input adj voltage) and (output adj	US-PGPUB;	
		voltage)	EPO; JPO;	
			DERWENT;	
			IBM_TDB	